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06CS46

Fourth Semester B.E. Degree Examination, January 2013
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the block diagram of connections between the processor and the memory, and explain how the following typical instructions can be executed with relevant steps :
i) Move NUM1, R_2
ii) Add R_3, NUM2. **(10 Marks)**

b. What is a bus? Explain the single bus structure used to interconnect functional units in computer system. **(04 Marks)**

c. Convert the following pairs of signed decimal number to 5 bit, signed, is complement binary numbers and add them. State whether over flow occurs or not in each case
i) 8 and 15
ii) – 12 and –2
iii) – 6 and 8. **(06 Marks)**

2 a. What is an addressing mode? Explain the following addressing modes, with an example for each :
i) Immediate addressing mode
ii) Indirect addressing mode
iii) Autoincrement addressing mode
iv) Relative addressing mode. **(10 Marks)**

b. For a simple example of I/O operations involving a key board and a display device, write an assembly language program that reads one line of characters from the key board, stores it in memory buffer and echoes it back to the display. **(05 Marks)**

c. What is stack? Explain its role in subroutine nesting. **(05 Marks)**

3 a. Explain the important functions of an I/O interface, with a neat block diagram. **(05 Marks)**

b. Explain with a neat diagram, how interrupt request from several I/O processor through a single INTR line. **(05 Marks)**

c. What is DMA? Explain the hardware registers that are required in a DMA controller chip. Explain the use of DMA controller in a computer system, with a neat diagram. **(10 Marks)**

4 a. With a neat block diagram, explain a general 8 – bit parallel interface circuit. **(10 Marks)**

b. Discuss the main phases involved in the operation of SCSI bus in detail, with an example. **(10 Marks)**

PART – B

5 a. Explain the synchronous DRAM, with the aid of a block diagram. **(10 Marks)**

b. With a simple arrangement of cache memory, explain how time required for main memory accesses can be reduced. **(06 Marks)**

c. Define Hit Rate and Miss Penalty. **(04 Marks)**

6 a. With a block diagram, explain the virtual memory organization. **(07 Marks)**
b. List and explain four major functions of disk controller. **(05 Marks)**
c. Explain the design of a 4 – bit carry – look ahead adder, with a neat diagram. **(08 Marks)**

7 a. Using a block diagram, which shows the register configuration, perform sequential circuit binary multiplication of multiplicand = 1010 and multiplier = 1101. **(08 Marks)**
b. Write and explain the algorithm for binary division using restoring division method, with an example. **(06 Marks)**
c. Explain the IEEE standard for floating point number representation. **(06 Marks)**

8 a. Briefly explain the single bus organization of the data path inside a processor, with a neat block diagram. **(08 Marks)**
b. Write and explain the control sequences for execution of following instruction, Add R_2, (R_4). **(06 Marks)**
c. Explain with neat block diagram, the basic organization of a microprogrammed control unit. **(06 Marks)**

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